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| 10/530,673 | 12/27/2005 | Michael Skerritt | A-10047 | 7710 |

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

| EXAMINER | |
|---|---|
| LEE, ANDREW CHUNG CHEUNG | |
| ART UNIT | PAPER NUMBER |
| 2419 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
sstiles@milesstockbridge.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/530,673 | SKERRITT, MICHAEL | |
| | Examiner | Art Unit | |
| | Andrew C. Lee | 2419 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. Claims 7 – 13 are newly added.

Claims 1 – 13 are pending.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Le Scolan et al. (US 7058729 B1).

**Regarding claim 1**, Le Scolan et al. disclose a system for transmitting a clock signal through a packet-based network *(Fig. 2, col. 10, lines 61 – 65)* comprising: a first node configured to measure a clock frequency of the clock signal and calculate an accuracy indicator of the measured clock frequency *("The first node having a counter monitoring clock pluses of a clock……,and "reading information…inserting at least said information or calculated information"; Fig.2, col. 5, lines 64 – 67, col. 6, lines 1 – 5)*, the accuracy indicator being a time duration of measurement *(Fig. 1, col. 3, lines 7 – 15)*; a second node configured to receive the clock frequency measurement and the accuracy indicator of the clock frequency measurement and configured to synthesize the clock

signal based on the clock frequency measurement and the accuracy indicator *("The second node having a counter monitoring clock pulses of a clock...., and reading information ….and reading synchronization information,,, and calculating a difference between information..."; Fig. 2, col. 6, lines 22 – 37, col. 3, lines 7 – 15)*; and a packet-based network to transmit the measured clock frequency and the accuracy indicator from the first node to the second node *(Fig. 2, col. 5, lines 59 – 67, col. 6, lines 1 – 2, lines 22 – 37)*.

**Regarding claim 8**, Le Scolan et al. disclose the system claimed wherein the second node is configured to receive one of a first indicator and a second indicator with the frequency measurement, the first indicator representing a first phase of operation for the second node, and the second indicator representing a second phase of operation for the second node, wherein, in the second phase of operation, the frequency of the synthesized clock signal is maintained ("determine a first term of information, determine a second term of information" as a first indicator and a second indicator with the frequency measurement; Fig. 6a - Fig. 6c, *col. 16, lines 57 – 67, col. 17, lines 1 – 57)*.

4. Claims 4, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Keating et al. (US 7099354 B2).

**Regarding claim 4**, Keating discloses in a packet-based network with a first transmitting node and a second receiving node *(Abstract, Fig. 1)*, a method of determining a frequency of a transmitting clock at the second receiving node *(Abstract, Fig. 3, col. 4, lines 57 – 65)*, said method comprising the steps of: receiving a first

plurality of packets *("After a predetermined number of timing packets has been received"; col. 4, lines 65 – 67, col. 5, lines 1 – 4)*; determining a total time for transmission for each packet *(col. 4, lines 57 – 66)*; identifying a first predetermined number of packets in the plurality of received packets that have the shortest total transmission times, the first predetermined number of packets identified being greater than one *("the lowest loopback delay value" interpreted as have the shortest total transmission times, "designated as twice the fixed or "nonblocked" Ethernet path delay.." as packets identified being greater than one; col. 4, lines 61 – 68, col. 5, lines 1 - 4)*; deriving the frequency of the transmitting clock by use of the identified first predetermined number of packets *(col. 5, lines 21 – 32).*

**Regarding claim 6**, Keating discloses the method claimed additionally comprising the steps of: identifying the packet in the first plurality of received packets that has the shortest total transmission time *("scan the payload field of the timing packet for a loopback delay measurement which corresponds to that period timing element 120"; Fig. 3, col. 4, lines 58 – 65)*; receiving a second plurality of packets; determining a total time for transmission for each packet in the second plurality of packets *(scan the payload field of the timing packet for a loopback delay measurement which corresponds to that period timing element 130 or 140"; Fig. 3, col. 4, lines 58 – 65 )*; identifying a second predetermined number of packets in the second plurality of received packets that have the shortest total transmission times *("the minimum loopback delay value detected will be designated"; col. 4, lines 65 – 68, col. 5, lines 1 – 4);* deriving the frequency of the transmitting clock through the identified second predetermined number

of packets in the second plurality of packets and the identified packet with the shortest total transmission time in the first plurality of packets *(col. 5, lines 21 – 32).*

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holden et al. (5255291) in view of Le Scolan et al. (US 7058729 B1).

**Regarding claim 2,** Holden et al. disclose a system for transmitting bit synchronous data through a packet-based network *(Abstract, col. 2, lines 43 – 47)* comprising: a first node configured to receive the bit synchronous data for transmission through the packet-based network, the first node including measurement hardware for generating a clock frequency measurement of the bit synchronous data and an accuracy indicator *("bit synchronous mode",..."frequency measurement using bit counters and system reference clocks,....., a very accurate low level indication of how close ...."; Fig. 2, col. 5, lines 55 – 60, col. 7, lines 10 – 61, col. 8, lines 50 – 64),*

Holden et al. do not disclose explicitly the clock frequency measurement and the accuracy indicator to be transmitted through the network; and, a second node configured to receive the clock frequency measurement and accuracy indicator from the first node via the packet-based network, and the second node including signal

synthesizer hardware to synthesize a clock signal from the clock frequency measurement and accuracy indicator to retrieve the bit synchronous data; wherein to generate the clock frequency measurement, the measurement hardware measures a number of counts during a predetermined period of time and the accuracy indicator is a period of time for measuring the number of counts.

Le Scolan et al. in the same field of endeavor teach the clock frequency measurement and the accuracy indicator to be transmitted through the network *(Fig. 2, col. 5, lines 59 – 64)*; and, a second node configured to receive the clock frequency measurement and accuracy indicator from the first node via the packet-based network, and the second node including signal synthesizer hardware to synthesize a clock signal from the clock frequency measurement and accuracy indicator to retrieve the bit synchronous data *("the apparatus having a counter monitoring clock pulses of a clock,….reading means for reading synchronizing information,….calculating means for calculating a difference between information…"; Fig. 2, col. 6, lines 38 – 53)*; wherein to generate the clock frequency measurement, the measurement hardware measures a number of counts during a predetermined period of time, and the accuracy indicator is a period of time for measuring the number of counts *("the circuits 214 and 240 of Fig. 3, Fig. 4" interpreted as the measurement hardware measures a number of counts during a predetermined period of time; col. 12, lines 62 – 67;, "the calculation unit" interpreted as the accuracy indicator; Fig. 6b, Fig. 6c, col. 16, lines 16 – 67)*.

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Holden et al. to include the features of

the clock frequency measurement and the accuracy indicator to be transmitted through the network; and, a second node configured to receive the clock frequency measurement and accuracy indicator from the first node via the packet-based network, and the second node including signal synthesizer hardware to synthesize a clock signal from the clock frequency measurement and accuracy indicator to retrieve the bit synchronous data; wherein to generate the clock frequency measurement, the measurement hardware measures a number of counts during a predetermined period of time and the accuracy indicator is a period of time for measuring the number of counts as taught by Le Scolan et al. One of ordinary skill in the art would be motivated to do so for a method of synchronization between communication networks exchanging information by frame of information, each communication network having clock and the number of clock pulses is monitored by a counter *(as suggested by Le Scolan et al., see col. 4, lines 66 – 67, col. 5, lines 1 – 2)*.

**Regarding 10,** Holden et al. disclose a system for transmitting bit synchronous data through a packet-based network *(Abstract, col. 2, lines 43 – 47)*. Holden et al. do not disclose explicitly wherein the second node is configured to receive a phase of operation indicator from the first node via the packet-based network, the phase operation indicator being one of a first phase of operation indicator and a second phase of operation indicator, wherein the second phase of operation indicator indicates that the clock frequency measurement received by the second node from the first node is accurate to a predetermined threshold.

Le Scolan et al. in the same field of endeavor teach wherein the second node is configured to receive a phase of operation indicator from the first node via the packet-based network, the phase operation indicator being one of a first phase of operation indicator and a second phase of operation indicator, wherein the second phase of operation indicator indicates that the clock frequency measurement received by the second node from the first node is accurate to a predetermined threshold *(determine a first term of information, determine a second term of information" as the phase operation indicator being one of a first phase of operation indicator and a second phase of operation indicator; Fig. 6a - Fig. 6c, col. 16, lines 57 – 67, col. 17, lines 1 – 57).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Holden et al. to include the features of wherein the second node is configured to receive a phase of operation indicator from the first node via the packet-based network, the phase operation indicator being one of a first phase of operation indicator and a second phase of operation indicator, wherein the second phase of operation indicator indicates that the clock frequency measurement received by the second node from the first node is accurate to a predetermined threshold as taught by Le Scolan et al. One of ordinary skill in the art would be motivated to do so for a method of synchronization between communication networks exchanging information by frame of information, each communication network having clock and the number of clock pulses is monitored by a counter *(as suggested by Le Scolan et al., see col. 4, lines 66 – 67, col. 5, lines 1 – 2).*

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Le Scolan et al. (US 7058729 B1) in view of Holden et al. (5255291).

**Regarding claim 3,** Le Scolan et al. disclose a method for adaptive clocking in a packet-based network between a first node and a second node *(Abstract )*, the method comprising the steps of: receiving a clock signal for transmission through the packet-based network at the first node *(reading information representing the counted clock pulses at the appearance of a reference event; col. 6, lines 1 – 2)*; measuring the clock signal to obtain a frequency measurement at the first node; determining an accuracy indicator for the measured frequency measurement at the first node, the *("The first node having a counter monitoring clock pluses of a clock……,and "reading information…inserting at least said information or calculated information"; Fig.2, col. 5, lines 64 – 67, col. 6, lines 1 – 5),* the accuracy indicator being a time duration of measurement *(Fig. 1, col. 3, lines 7 – 15)*; transmitting the frequency measurement and the accuracy indicator through the packet-based network from the first node to the second node *(Fig. 2, col. 5, lines 59 – 64)*; receiving the frequency measurement and the accuracy indicator at the second node; deriving a clock signal from the frequency measurement and the accuracy indicator at the second node *("the apparatus having a counter monitoring clock pulses of a clock,….reading means for reading synchronizing information,….calculating means for calculating a difference between information…"; Fig. 2, col. 6, lines 38 – 53)*; and Le Scolan et al. do not disclose explicitly transmitting the derived signal from the second node to a user equipment connected to the second node.

Holden et al. in the same field of endeavor teach transmitting the derived signal from the second node to a user equipment connected to the second node *("User equipment DTE connecting to IPX"; Fig. 4, col. 10, lines 22 – 33).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Le Scolan et al. to include the features of teach transmitting the derived signal from the second node to a user equipment connected to the second node as taught by Holden et al. One of ordinary skill in the art would be motivated to do so for providing an improved clocking transmission system and method for use in a communication system *(as suggested by Holden et al., see col. 1, lines 60 – 62).*

**Regarding claims 7, 9,** Le Scolan et al. disclose the synthesis includes the accuracy indicator *("The first node having a counter monitoring clock pluses of a clock……,and "reading information…inserting at least said information or calculated information"; Fig.2, col. 5, lines 64 – 67, col. 6, lines 1 – 5).* Le Scolean et al. do not disclose wherein the synthesis includes multiplying the clock frequency measurement by the accuracy indicator

Holden et al. in the same field of endeavor teach wherein the synthesis includes multiplying the clock frequency measurement by the accuracy indicator *(Abstract, Fig. 6, Fig. 7, col. 7, lines 10 – 67, col. 8, lines 1 – 24).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Le Scolan et al. to include the features of wherein the synthesis includes multiplying the clock frequency measurement by the

accuracy indicator as taught by Holden et al. One of ordinary skill in the art would be motivated to do so for providing an improved clocking transmission system and method for use in a communication system *(as suggested by Holden et al., see col. 1, lines 60 – 62)*.

**Regarding claim 11,** Le Scolan et al. disclose the system claimed wherein said transmitting further includes transmitting a phase indicator through the packet-based network from the first node to the second node, wherein the phase indicator is one of a first phase indicator and a second phase indicator, wherein the first phase indicator indicates capturing and recovering of the clock signal, and wherein the second phase indicator indicates maintaining the clock signal *(determine a first term of information, determine a second term of information" as transmitting a phase indicator through the packet-based network from the first node to the second node, wherein the phase indicator is one of a first phase indicator and a second phase indicator; Fig. 6a - Fig. 6c, col. 16, lines 57 – 67, col. 17, lines 1 – 57)*.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keating (US 7099354 B2) in view of Mauritz et al. (US 6658025 B2).

**Regarding claim 5**, Keating discloses in a packet-based network with a first transmitting node and a second receiving node *(Abstract, Fig. 1)*. Keating does not disclose explicitly the method claimed wherein the derived frequency is used to maintain buffer fill at the second receiving node.

Mauritz et al. in the same field of endeavor teach the method claimed wherein the derived frequency is used maintain buffer fill at the second receiving node *("to estimate the frequency f using advantageously a pre-defined window of time stamps"; col. 4, lines 32 – 43; col. 3, lines 64 – 66).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Keating to include the features of teach transmitting the derived signal from the second node to a user equipment connected to the second node as taught by Mauritz et al. One of ordinary skill in the art would be motivated to do so for providing enhancement of frequency synchronization in networks with variable delays *(as suggested by Mauritz et al., see col. 1, lines 51 – 22).*

9. Claims 12, 13 are rejected under 35 U.S.C. 103(a) as being being unpatentable over Keating et al. (US 7099354 B2) in view Yun et al. (US 20020176362 A1).

**Regarding claims 12, 13,** Keating discloses in a packet-based network with a first transmitting node and a second receiving node *(Abstract, Fig. 1)*, a method of determining a frequency of a transmitting clock at the second receiving node *(Abstract, Fig. 3, col. 4, lines 57 – 65)*, Keating does not disclose explicitly wherein the first predetermined number of packets identified is three, and wherein the second predetermined number of packets identified is three.

Yun et al. in the same field of endeavor teach wherein the first predetermined number of packets identified is three, and wherein the second predetermined number of packets identified is three *("the delay time of the three packet'; para. [0198]).*

At time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the teachings of Keating to include the features of wherein the first predetermined number of packets identified is three, and wherein the second predetermined number of packets identified is three as taught by Yun et al. One of ordinary skill in the art would be motivated to do so for providing a mthod of retransmitting data through a reverse link in a packet data system using ARQ (Automatic Repeat Request) *(as suggested by Yun et al., see para. [0003]).*

***Response to Arguments***

10. Applicant's arguments filed on 01/26/2009 with respect to claims 1 – 6 have been fully considered but they are not persuasive.

Regarding claim 2, applicant argues reference Le Scolan fails to teach a first node including measurement hardware to generate a clock frequency measurement of the bit synchronous data and an accuracy indicator, wherein the accuracy indicator is a period of time for measuring the number of counts. Examiner respectfully disagrees.

Examiner contends the combined system of references Holden and Le Scolan discloses a first node including measurement hardware to generate a clock frequency measurement of the bit synchronous data and an accuracy indicator, wherein the accuracy indicator is a period of time for measuring the number of counts. Examiner interpreted a first node including measurement hardware to generate a clock frequency measurement of the bit synchronous data as "bit synchronous mode",..."frequency measurement using bit counters and system reference clocks,....., a very accurate low

level indication of how close ...."; see Holden, Fig. 2, col. 5, lines 55 – 60, col. 7, lines 10 – 61, col. 8, lines 50 – 64, and interpreted wherein the accuracy indicator is a period of time for measuring the number of counts as "the circuits 214 and 240 of Fig. 3, Fig. 4" interpreted as the measurement hardware measures a number of counts during a predetermined period of time; see Le Scolan, col. 12, lines 62 – 67;, "the calculation unit" interpreted as the accuracy indicator; Fig. 6b, Fig. 6c, col. 16, lines 16 – 67.

Regarding claim 4, Applicant then argues reference Keating fails to teach or suggest identifying a first predetermined number of packets in a plurality of received packets that have the shortest total transmission times, the first predetermined number of packets identified being greater than one. Examiner respectfully disagrees.

Examiner contends reference Keating disclose identifying a first predetermined number of packets in a plurality of received packets that have the shortest total transmission times, the first predetermined number of packets identified being greater than one. Examiner interpreted identifying a first predetermined number of packets in a plurality of received packets that have the shortest total transmission times as "the lowest loopback delay value" and predetermined number of packets identified being greater than one, "designated as twice the fixed or "nonblocked" Ethernet path delay.." see Keating, col. 4, lines 61 – 68, col. 5, lines 1 – 4.

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Matsumoto et al. (4845709).
b) Roust (US 6829717 B1).

c) Raisanen et al. (US 6577648 B1).

d) Trans (US 6377640 B2).

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571)272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew C Lee/
Examiner, Art Unit 2419
<3/31/2009::3Qy09>

/Edan Orgad/
Supervisory Patent Examiner, Art Unit 2419